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GB 2274739 A US 5631571 A

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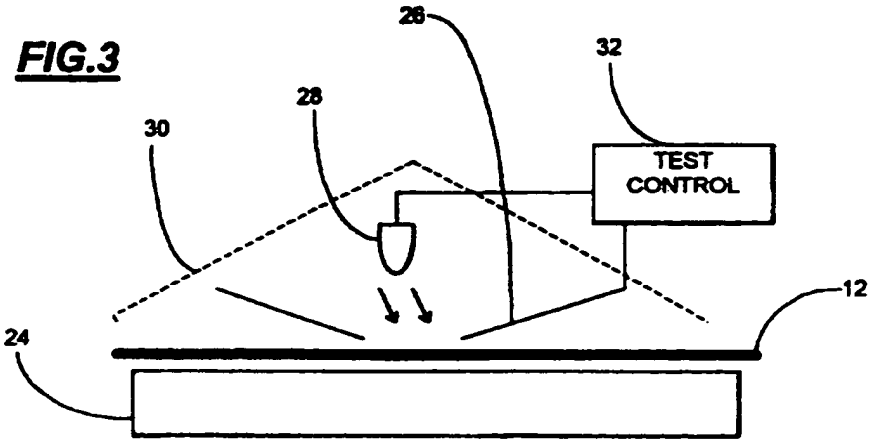
(54) Abstract Title
Testing optical/electronic integrated circuits

(57) Test apparatus for testing the optical and electronic functionality of an integrated circuit die, prior to packaging, comprises a movable chuck 24 for supporting and locating a wafer containing one or more dies; probe pins 26 for electrically contacting the die; and an optical source 28 for illuminating a test area of the die with an optical signal. In one form the optical signal may represent an optical clock for simulating optical clocking of the die when mounted in a package containing an off chip light emitter. One or more lenses may be provided to focus the light on the surface of the die, or the light may be directed onto the surface of the die by reflectors. A light shield 30 may be provided during testing to protect the device under test from ambient light. "Light" may be interpreted as visible, infra red or ultra violet radiation.

FIG.3



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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

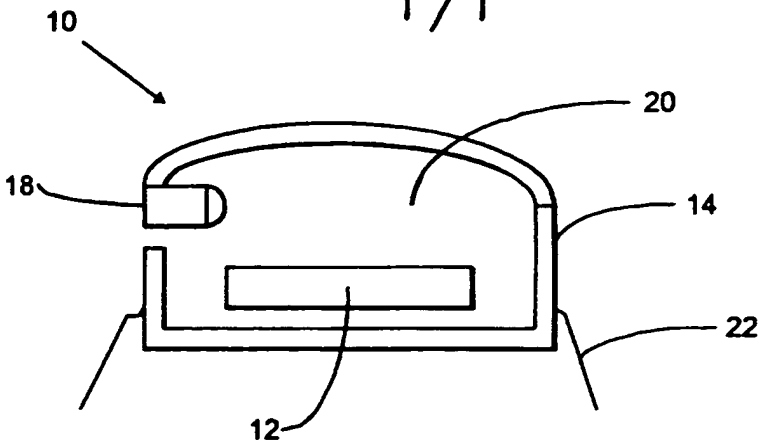

FIG. 1

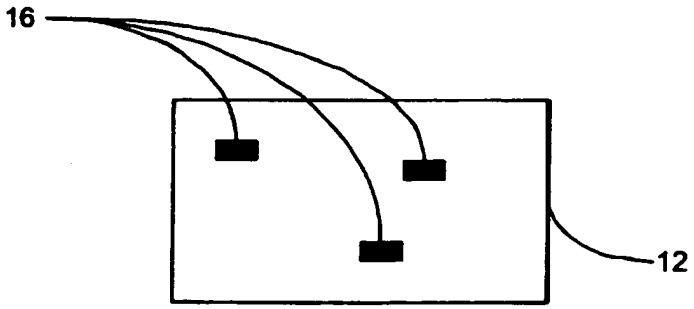

FIG. 2

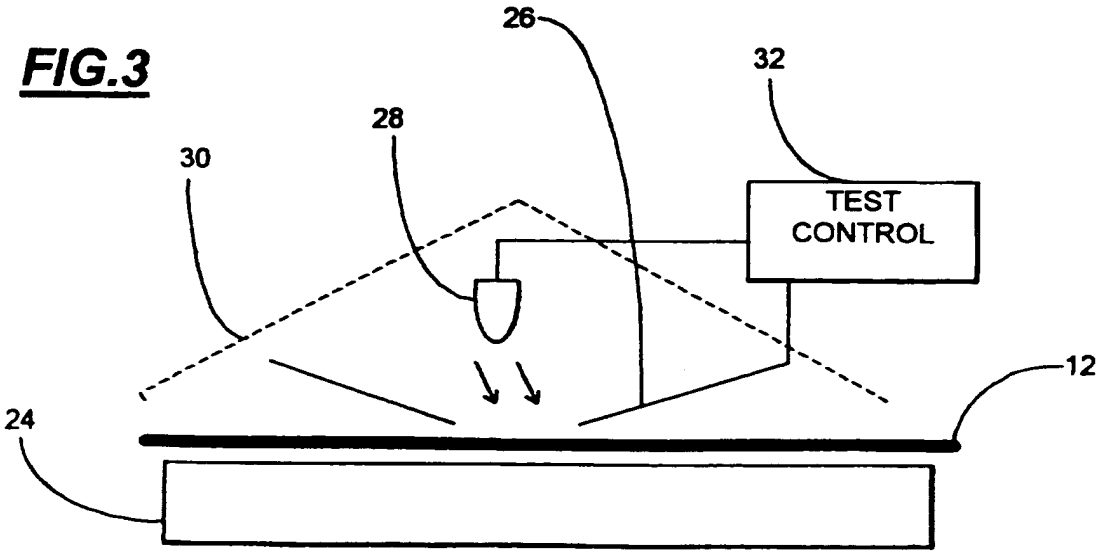

FIG.3

METHOD APPARATUS FOR TESTING OPTICAL/ELECTRONIC INTEGRATED CIRCUITS

This invention relates to testing integrated circuits which include electronic signal inputs and one or more optical inputs. The technique is especially suitable for testing integrated circuit dies which receive optical signals not generated on the die itself. For example, co-pending UK application no. 9712177.6 entitled Low Skew Signal Distribution of Integrated Circuits describes an integrated circuit die which is clocked by an off-chip source mounted within the package. Such optical clocking can provide very low skew across the die, and the amount of skew is not dependent on stray capacitive effects which are difficult to predict.

In contrast to existing electronic testing techniques, one aspect of the invention is to enable functional testing of an integrated circuit die having both electrical and optical inputs, prior to packaging the die. In accordance with the principles of the invention, one or more test connectors are used to provide electronic connections to the die, and an optical source is provided to illuminate the die with an optical signal.

In developing the invention, it was appreciated that existing techniques for testing integrated circuit dies can only be used to test an optically sensitive die if additional parallel circuitry is incorporated in the die to permit injection of electronic clock signals. However such parallel circuitry would occupy valuable chip space. Moreover, an electronic-only test does not provide a comprehensive testing of the optical receivers in the die.

In a specific aspect, the invention provides test apparatus comprising means for supporting and locating an integrated circuit wafer containing one or more circuit dies, means for contacting one or more areas of the wafer to apply signals to and/or to receive electronic signals therefrom, and optical means for illuminating at least a test area of the wafer with an optical signal.

In a closely related aspect, the invention provides a method of testing an electronic/optical integrated circuit die, the method comprising contacting the die with one or more electrical contacts for applying electronic signals to the die and/or for

receiving electronic signals from the die, and illuminating at least a test area of the die with an optical signal.

The term "optical" as used herein is not limited only to visible light, but refers to any electromagnetic radiation which substantially obeys the laws of optics. The terms includes, but is not limited to, infra red light, visible light, and ultra-violet light.

In a preferred form, the optical signal is modulated to represent an optical clock signal incident on the die.

An embodiment of the invention is now described by way of example only, with reference to the accompanying drawings, in which:-

Fig. 1 is a schematic side section showing an optically clocked integrated circuit installed in its package;

Fig. 2 is a schematic plan view showing photosensitive areas on the surface of the die; and

Fig. 3 is a schematic diagram illustrating an electronic and optical test apparatus.

Referring to Figs. 1 and 2, the structure of an optical integrated circuit 10 is first described briefly. The integrated circuit 10 is generally as illustrated in the aforementioned UK application no. 9712177.6, and comprises a semiconductor die 12 mounted on a package base 14. The upper surface of the die 12 has a number of photo-sensitive regions or windows 16 for receiving an optical clock signal from an off-chip LED source 18 mounted in the package. The region above the die 12 is filled with optically translucent material 20, and is topped with an opaque cover to prevent the optical interference from ambient light or between adjacent integrated circuit packages. The LED source 18 is driven by an electronic signal applied through particular ones of the package pins 22. The remaining pins form conventional connections (not shown) to the die 12.

Fig. 3 illustrates test apparatus capable of testing the electronic and optical functionality of the die 12 prior to packaging. The apparatus comprises a movable chuck support 24 for supporting and locating a wafer containing one or more dies to be tested. Above the chuck 24 is positioned a set of probe card pins 26 for forming direct

electrical contacts to the pads of the die (for clarity only two pins 26 are illustrated in Fig. 3).

The test apparatus further includes an optical source 28 positioned to illuminate the region of the wafer under test. Although not shown in he figure, one or more lenses may be provided to focus the light on to the surface of the wafer. Additionally, or alternatively, if the source is not positionable in line of sight of the wafer surface, one or more reflectors may be provided to reflect the light to the wafer surface. The source may comprise any suitable source generating sufficient incident light, and being modulatable to simulate an optical modulation signal. Suitable devices include LED's (either single high brightness types or arrays of LED's), lasers, etc. The light is preferably of about the same wavelength as that of the package source 18, but any wavelength known to be photodetectable by the die's optical receivers may be used.

As depicted by the broken line 30, a cover or shield may be provided to isolate the die from the effects of ambient light (or at least to reduce the effect of ambient light).

The pins 26 and the source 28 are driven by a test control circuit depicted schematically by numeral 32. The test circuit is similar to conventional test circuits, but includes additional circuitry, as necessary, to drive the optical source 28.

It will be appreciated that the invention, particularly as described in the preferred embodiment, can provide comprehensive testing of the optical and electronic functionality of an optical/electronic integrated circuit. If the die is found to be faulty, either optically or electronically, then the die can be discarded, thus saving the cost of the package and of the built-in light source. The invention is especially suitable when the die is intended to be mounted directly on a circuit board as a so-called "chip on board" without being first mounted in a package; such an implementation requires full testing of the integrated circuit before the die is mounted on the circuit board.

The invention is also particularly suitable for enabling testing of integrated circuit dies intended to receive signals from one or more off-chip optical sources.

It will be appreciated that the above description is merely illustrative, and that many modifications may be made within the scope and/or principles of the invention.

features believed to be of particular importance are recited in the appended claims. However, the Applicant claims protection for any novel feature or combination of features described herein and/or illustrated in the drawings, irrespective of whether emphasis is placed thereon.

CLAIMS

1. Apparatus for testing electronic and optical functionality of an integrated circuit having one or more electrical contact areas, and one or more optical receivers areas, the apparatus comprising:

means for establishing one or more electrical contacts to the die; and

optical means for illuminating at least a test area of the die with an optical signal.

2. Apparatus according to claim 1, further comprising means for supporting and locating the die, or a wafer containing the die.

3. Apparatus according to claim 1 or 2, further comprising means for controlling modulation of the optical source.

4. Apparatus according to claim 1, 2 or 3, further comprising means for focusing light from the source on to the surface of the die.

5. Apparatus according to any preceding claim, wherein the electrical contact means comprise probe card pins for contacting contact pads on the die.

6. A method of tesfing electronic and optical functionality of an integrated circuit having one or more electrical contact areas and one or more optical receivers, the method comprising:

contacting the die with one or more contacts for establishing electrical connections to the die; and

illuminating at least a test area of the die with an optical signal.

7. A method according to claim 6, wherein the optical signal is generated as a modulated signal representing an optical clock signal.

8. Test apparatus, or a test method, substantially as hereinbefore described with reference to Fig. 3 of the accompanying drawings.

The Patent Office

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Application No: GB 9727281.9 **Examiner:** Miss E.L.Rendle
Claims searched: 1-8 **Date of search:** 25 March 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H1K (KMA); H4B; G1U (UR)

Int Cl (Ed.6): H01L; G01R

Other: Online :WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2 274 739 A	(MITSUBISHI) see figure 7 and page 10 line 11 to page 11 line 14.	1, 2, 3, 5, 6
X	US 5 631 571 A	(US AIR FORCE) see whole document.	1, 3, 4, 5, 6

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.